What is Claimed is:

[c1] An integrated circuit device, comprising:

a first power rail for supplying power to first latch and a circuit during a first clock phase;

a second power rail for supplying power to a second latch during a second clock phase; and

said circuit coupled between an output of said first latch and an input of said second latch.

[c2] The integrated circuit device of claim 1, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

[c3] The integrated circuit device of claim 1,wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks powered from a third power rail.

[c4] The integrated circuit device of claim 1, wherein:

said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low; and

said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low.

[c5] The integrated circuit device of claim 1, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

[c6] An integrated circuit device, comprising:

a first power rail for supplying power to an L1 latch of an L1/L2 latch during a first clock phase; and

a second power rail for supplying power to an L2 latch of said L1/L2 latch and to a circuit coupled to an output of said L2 latch during a second clock phase.

[c7] The integrated circuit device of claim 6, further comprising a second L1/L2 latch wherein said circuit is coupled to an input of an L1 latch of said second L1/L2 latch, said L1 latch of said second L1/L2 latch powered by said first power rail

and an L2 latch of said second L1/L2 latch powered by said second power rail.

[c8] The integrated circuit device of claim 6,wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks powered from a third power rail.

[c9] The integrated circuit device of claim 6, wherein:

said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low; and

said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low.

[c10] The integrated circuit device of claim 6, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

[c11] An integrated circuit device, comprising:

a first power rail for supply power to first latch and a first circuit during a first clock phase;

a second power rail for supplying power to a second latch and a second circuit during a second clock phase;

a third power rail for supplying power to a third latch and a third circuit during a third clock phase;

a fourth power rail for supply power to fourth latch and a fourth circuit during a fourth clock phase; and

said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch.

[c12] The integrated circuit device of claim 11, further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

[c13] The integrated circuit device of claim 11,wherein said first clock phase is

supplied from a first clock, said second clock phase is supplied from a second clock, said third clock phase is supplied from a third clock and said fourth clock phase is supplied from a fourth clock, said first, second, third and fourth clocks powered from a fifth power rail.

[c14] The integrated circuit device of claim 11, wherein:

said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low;

said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low;

said third power rail is powered before said third clock phase goes high and is de-powered after said third clock phase goes low; and

said fourth power rail is powered before said fourth clock phase goes high and is de-powered after second first clock phase goes low.

[c15] The integrated circuit device of claim 11, wherein only one of said first clock phase, second clock phase, third clock phase and fourth clock phase is high at a time.

[c16] The integrated circuit of claim 15, wherein said second clock phase goes high when said first clock phase goes low, said third clock phase goes high when said second clock phase goes low, said fourth clock phase goes high when said third clock phase goes low and said first clock phase goes high when said fourth clock phase goes low.

[c17] A method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supplying power to first latch and a circuit, a second power rail for supplying power to a second latch, and said circuit coupled between an output of said first latch and an input of said second latch, comprising:

powering said power rail during each phase of a first clock; and

powering said second power rail each phase of a second clock.

[c18] The method of claim 17, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

[c19] The method of claim 17,wherein:

said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock; and

powering said first and second clocks from a third power rail.

[c20] The method of claim 17, further including:

powering said first power rail before said first clock phase goes high and de-powering said first power rail after said first clock phase goes low; and

powering second power rail before said second clock phase goes high and de-powering said second rail after second first clock phase goes low.

[c21] The method of claim 17, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

[c22] A method of stressing an integrated circuit device, said integrated circuit device including a first power rail for supplying power to an L1 latch of an L1/L2 latch; and a second power rail for supplying power to an L2 latch of said L1/L2 latch and to a circuit coupled to an output of said L2 latch, comprising:

powering said first power rail during each phase of a first clock; and

powering said second power rail during each phase of a second clock.

[c23] The method of claim 22, said circuit further comprising a second L1/L2 latch, said circuit coupled to an input of an L1 latch of said second L1/L2 latch, said L1 latch of said second L1/L2 latch powered by said first power rail and an L2 latch of said second L1/L2 latch powered by said second power rail.

[c24] The method of claim 22,wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks are powered from a third power rail.

[c25] The method of claim 22, further including:

powering said first power rail before said first clock phase goes high and de-powering said first power rail after said first clock phase goes low; and

powering said second power rail before said second clock phase goes high and de-powering said second power rail after second first clock phase goes low.

[c26] The method of claim 22, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

[c27] A method of stressing an integrated circuit device, said integrated circuit device including a first power rail for supply power to first latch and a first circuit, a second power rail for supplying power to a second latch and a second circuit, a third power rail for supplying power to a third latch and a third circuit, a fourth power rail for supply power to fourth latch and a fourth circuit, and said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch, comprising:

powering said first power rail during each phase of a first clock;
powering said second power rail during each phase of a second clock;
powering said third power rail during each phase of a third clock; and
powering said fourth power rail during each phase of a fourth clock.

[c28] The method of claim 27, said integrated circuit further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

[c29] The method of claim 27,wherein:

said first clock phase is supplied from a first clock, said second clock phase is supplied from a second clock, said third clock phase is supplied from a third clock and said fourth clock phase is supplied from a fourth clock; and
powering said first, second, third and fourth clocks from a fifth power rail.

[c30] The method of claim 27, further including:

powering said first power rail before said first clock phase goes high and de-powering said first power rail after said first clock phase goes low;

powering said second power rail before said first clock phase goes high and de-powering said second power rail after said first clock phase goes low;

powering said third power rail before said first clock phase goes high and de-powering said third power rail after said first clock phase goes low; and

powering said fourth power rail before said first clock phase goes high and de-powering said fourth power rail after said first clock phase goes low.

[c31] The method of claim 27, wherein said only one of said first clock phase, said second clock phase, said third clock phase and fourth clock phase is high at a time.

[c32] The method of claim 31, wherein said second clock phase goes high when said first clock phase goes low, said third clock phase goes high when said second clock phase goes low, said fourth clock phase goes high when said third clock phase goes low and said first clock phase goes high when said fourth clock phase goes low.